REMARKS

Applicant amends claims 1, 7, 10, 11, and 18, and cancels claims 6, 9, and 17. Applicant submits that no new matter has been introduced by amendments to claims 1, 7, 10, 11, and 18. Claims 1 and 11 have been amended to include elements of claims 9 and 17, respectively. Claims 7, 10, and 18 have been amended to correct references to canceled claims accordingly. Claims 1-5, 7-8, 10-16, 18-21 are now pending in this application.

Please associate this application with Customer Number 22,852. Also, please address all correspondence with respect to this application to:

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If there is any fee due in connection with the filing of this Preliminary Amendment, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

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Dated: August 23, 2002

By: _____
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APPENDIX

1. A secure processing unit[, the secure processing unit including] comprising:

an internal memory unit;

a processor;

tamper detection and response logic;

an interface to external systems or components;

one or more buses for connecting the internal memory unit, the processor, the tamper detection and response logic, and the interface to external systems and components;

a memory management unit;

a level-one page table, the level-one page table including a plurality of level-one page table entries, wherein the level-one page table entries each correspond to at least one level-two page table, and wherein the level-one page table entries each contain a predefined attribute, the predefined attribute being operable to indicate to the memory management unit whether entries in a corresponding level-two page table may designate certain predefined memory regions;

a plurality of processor security registers; and

a tamper-resistant housing.

7. A secure processing unit as in claim [6, including] 1, further comprising:

access control data, the access control data being operable to indicate whether access to predefined memory regions is restricted to certain software components or processor modes.

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10. A secure processing unit as in claim [9] 1, whereby level-two page tables that may not designate the predefined memory regions are not stored in the internal memory unit.

11. An information appliance[, the information appliance] comprising:

a memory unit;

a secure processing unit[, the secure processing unit including] comprising:

a tamper resistant packaging[;],

tamper detection and response logic[;],

a secure memory unit[;], and

a processing unit, including a memory management unit and a plurality of processor security registers;

a level-one page table and a plurality of level-two page tables, the level-one page table including a plurality of level-one page table entries and the level-two page table including a plurality of level-two page table entries, wherein the level-one page table entries each correspond to at least one level-two page table, and wherein the level-one page table entries each contain a predefined attribute, the predefined attribute being operable to indicate to the memory management unit whether a corresponding level-two page table may designate certain predefined memory regions; and

a bus for connecting the memory unit and the secure processing unit;

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wherein the secure processing unit is operable to perform both secure processing operations and at least some processing operations performed by a conventional information appliance processing unit.

18. An information appliance as in claim [17] 11, in which level-two page tables that may not designate the predefined memory regions are stored in the memory unit, and wherein the level-one page table and the level-two page tables that may designate the predefined memory regions are stored in the secure memory unit.

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